REMARKS

Claims 1-2, 8-11, 13-14, 17-18, and 20-37 remain pending. Applicants note that claim 12 was cancelled in the Response mailed March 23, 2004 (received in the PTO on March 26, 2004 -- referred to herein as the "previous Response"). The summary sheet of the Office Action appears to indicate that claim 12 is still pending, although the Office Action contents do not contain a specific rejection of claim 12. In the present Office Action, claims 1-2, 8-11, 13-14, 17-18, 20-32, and 35 were rejected under 35 U.S.C. § 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992 ("Killian"). Claims 33 and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Killian in view of IEEE. Claims 34 and 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Killian in view of Hennesey (Computer Architecture). Applicants respectfully traverse these rejections and request reconsideration.

Section 102/103 Rejections

Applicants respectfully submit that each of claims 1-2, 8-11, 13-14, 17-18, and 20-37 recites a combination of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "said execution core is configured to zero extend said result for update in said register responsive to *an operand size corresponding to said instruction specifying* a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to *said operand size [corresponding to said instruction] specifying* a third number of bits less than said first number of bits and different from said second number". Applicants have added [corresponding to said instruction] above merely to further highlight the patentability of claim 1 over Killian. The antecedent basis of "said operand size" makes it clear that is the same operand size (and instruction) referred to earlier in the claim.

The Office Action alleges that Killian anticipates the above highlighted features. However, the Office Action cites two separate and distinct instructions from Killian to allegedly teach the above features. Specifically, the Office Action uses the LBU (load byte unsigned) instruction to allegedly teach "said execution core is configured to zero

extend said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits" and the ORI (logical OR immediate) instruction to allegedly teach "said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits".

These two separate instructions cannot anticipate "said execution core is configured to zero extend said result for update in said register responsive to *an operand size corresponding to said instruction specifying* a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to *said operand size [corresponding to said instruction] specifying* a third number of bits less than said first number of bits and different from said second number". Applicants respectfully submit that Killian does not teach or suggest an execution core having the above features.

For at least the above stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 2 and 8-11, being dependent from claim 1, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 2 and 8-11 recites additional combinations of features not taught or suggested in the cited art.

Claim 13 recites a combination of features including: "zero extending said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits; and preserving a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number." The same teachings of Killian highlighted above with regard to claim 1 are also alleged to teach the above highlighted combination of features of claim 13. Applicants respectfully submit that the teachings of Killian do not anticipate the above highlighted features of claim 13 either, for reasons similar to those given above. Accordingly, Applicants submit that claim 13 is patentable

over the cited art. Claims 14 and 17-18, being dependent from claim 13, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 14 and 17-18 recites additional combinations of features not taught or suggested in the cited art.

Claim 20 recites a combination of features including: "said execution core is configured to zero extend said result for update in said storage location responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution circuit is configured to preserve a value of at least a portion of said bits in said storage location that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number". The same teachings of Killian highlighted above with regard to claim 1 are also alleged to teach the above highlighted combination of features of claim 20. Applicants respectfully submit that the teachings of Killian do not anticipate the above highlighted features of claim 20 either, for reasons similar to those given above. Accordingly, Applicants submit that claim 20 is patentable over the cited art. Claims 21-25, being dependent from claim 20, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 21-25 recites additional combinations of features not taught or suggested in the cited art.

Claim 26 recites a combination of features including "said execution core is configured to extend said result to said first number of bits for update in said storage location responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution circuit is configured to preserve a value of at least a portion of said bits in said storage location that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number". The same teachings of Killian highlighted above with regard to claim 1 are also alleged to teach the above highlighted combination of features of claim 26. Applicants respectfully submit that the teachings of Killian do not anticipate the above highlighted features of claim 26 either, for reasons similar to those given above. Accordingly, Applicants submit that claim 26 is patentable over the cited art. Claims 27-

31, being dependent from claim 26, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 27-31 recites additional combinations of features not taught or suggested in the cited art.

Claim 32 recites a combination of features including "said execution core is configured to zero extend said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number". The same teachings of Killian highlighted above with regard to claim 1 are also alleged to teach the above highlighted combination of features of claim 32. Applicants respectfully submit that the teachings of Killian do not anticipate the above highlighted features of claim 32 either, for reasons similar to those given above. Accordingly, Applicants submit that claim 32 is patentable over the cited art. Claims 33-34, being dependent from claim 33, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 33-34 recites additional combinations of features not taught or suggested in the cited art.

Claim 35 recites a combination of features including "said execution core is configured to extend said result to said first number of bits for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number". The same teachings of Killian highlighted above with regard to claim 1 are also alleged to teach the above highlighted combination of features of claim 35. Applicants respectfully submit that the teachings of Killian do not anticipate the above highlighted features of claim 35 either, for reasons similar to those given above. Accordingly, Applicants submit that claim 35 is patentable over the cited art. Claims 36-37, being dependent from claim 35,

are similarly patentable over the cited art for at least the above stated reasons. Each of claims 36-37 recites additional combinations of features not taught or suggested in the cited art.

Comments on item 41 in Office Action

Item 41 (page 23) of the Office Action states "The examiner notes on the record that no arguments have been entered regarding the limitations not inherited by the parent claims for claims 2, 8-11, 14, and 17-18". Applicants respectfully disagree. For example, the previous Response states "Each of claims 2 and 8-11 recites additional combinations of features not taught or suggested in the cited art." (previous Response, page 10, first paragraph). Similar language can be found elsewhere in the previous Response for the other dependent claims.

Given the patentability of the independent claims over the cited art (as explained above), there is no need to present detailed additional arguments for the dependent claims at this time. However, Applicants do not concede that the features recited in the dependent claims are taught in the cited art as alleged in the Office Actions, as highlighted by the traversal of all rejections in the previous Response and the present Response, as well as by the above highlighted language. Specifically, Applicants reserve the right to advance such additional detailed arguments, such as during an appeal before the Board of Patent Appeals and Interferences.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-64000/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Please charge the above-identified deposit account in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,

Lawrence J. Merkel
Reg. No. 41,191
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: 7/9/04